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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,739	OKAMOTO ET AL.	
	Examiner	Art Unit	
	SARAH K. SALERNO	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 15-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 15-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/6/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment/arguments filed on 07/02/09 as being acknowledged and entered. By this amendment claims 13 and 14 are canceled, claims 22 and 23 have been added claims 1-12 and 15-23 are pending and no claims are withdrawn.

2. The rejection of claims 1-12 and 15-21 in the Non-Final office action dated 03/04/09 are withdrawn based on applicants amendments.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 contains the limitation "the drain electrode side of said insulating film is made of an insulating material containing silicon and nitrogen as constituent elements". The claim limitation uses the term "containing" which means no other elements can be in the insulating film other than silicon and nitrogen. Claim 11, however, depends on claim 10 and its limitation adds oxygen as one of the constituent elements in the drain electrode side of said insulating film. Claim 11 is therefore unclear and is being interpreted as the gate electrode side of the insulating film contains silicon, nitrogen and oxygen.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3, 5, 6, 8, 10-12, 15 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Green et al. (US Patent 6,867,078).

Claim 1: Green teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) (18) and an electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$) (14), a source electrode (30) and a drain electrode (30) formed on the semiconductor layer structure while being separated from each other, a gate electrode (44) arranged between said source electrode and said drain electrode, and an insulating film (32,34) formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion (above 36) formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode and said insulating film is a multilayered film including a first insulating film (32) and a second insulating film (34), said first insulating film being made of a compound containing silicon and nitrogen as constituent elements,

said second insulating film having a dielectric constant lower than that of said first insulating film (FIG. 8; ABS, Col. 2 lines 20-67]).

Claim 2: Green teaches the second insulating film is laminated on said first insulating film (FIG. 8).

Claim 3: Green teaches the thickness of said first insulating film is not more than 150 nm (FIG. 8).

Claim 5: Green teaches said insulating film including said multilayered film is formed while being separated from said gate electrode, and said second insulating film is provided between said first insulating film and said gate electrode (FIG. 8).

Claim 6: Green teaches said second insulating film is provided between said first insulating film and said gate electrode and said second insulating film is positioned below said field plate portion, and said multilayered film including said first insulating film and said second insulating film is positioned between a drain-side end portion of said field plate portion and said drain electrode (FIG. 8).

Claim 8: Green teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including: a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) (18) and an electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$) (14), a source electrode (30) and a drain electrode (30) formed on the semiconductor layer structure while being separated from each other, a gate electrode (44) arranged between said source electrode and said drain electrode, and an insulating film (32,34) formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion (above 36) formed on said insulating film while said field plate portion

has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode and said insulating film (32, 34) is made of a compound containing silicon, nitrogen and oxygen as constituent elements (FIG. 8; ABS, Col. 2 lines 20-67]).

Claim 10: Green teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including: a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) (18) and an electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$) (14), a source electrode (30) and a drain electrode (30) formed on the semiconductor layer structure while being separated from each other, a gate electrode (44) arranged between said source electrode and said drain electrode, and an insulating film (32, 34) formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion (above 36) formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode and said gate electrode side of said insulating film between said gate electrode and said drain electrode is made of an insulating material (34) having dielectric constants not more than 4, and said drain electrode side of said insulating film is made of an insulating material (32) containing silicon and nitrogen as constituent elements (FIG. 8; ABS, Col. 2 lines 20-67]).

Claim 11: Green teaches the gate electrode side of said insulating film is made of an insulating material containing silicon, nitrogen, and oxygen as the constituent elements (32) (FIG. 8; ABS, Col. 2 lines 20-67]).

Claim 12: Green teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) (18) and an electron supply layer $Al_yGa_{1-y}N$ ($0 < y \leq 1$) (14), a source electrode (30) and a drain electrode (30) formed on the semiconductor layer structure while being separated from each other, a gate electrode (44) arranged between said source electrode and said drain electrode, and an insulating film (32,34) formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion (above 36) formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode and the drain electrode side is lower than said gate electrode side in a dielectric constant of a capacity formed by said field plate portion, said Group III nitride semiconductor layer, and said insulating film sandwiched therebetween,

wherein a part of said insulating film is a multilayered film including a first insulating film (32) and a second insulating film (34), said first film being made of a compound containing silicon and nitrogen as constituent elements, said second insulating film having a dielectric constant lower than that of said first insulating film, and said gate electrode side is formed by a single layer film of the first insulating film (32) and said drain electrode side is formed by the multilayered film including said first insulating film and said second insulting film in said insulating film between said field plate portion and a surface of said semiconductor layer structure (FIG. 8; ABS, Col. 2 lines 20-67]).

Claim 15: Green teaches contact layers (28,29) are arranged between said source electrode and a surface of said semiconductor layer structure and between said drain electrode and a surface of said semiconductor layer structure, respectively (Fig. 8).

Claim 17: Green teaches the field plate portion extends to an upper portion of said contact layer (Fig. 8).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-4, 8-12, 18, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (US PGPub 2001/0015446 of record) in view of Mayuzumi (US PGPub 2002/0079525).

Claim 1: Inoue teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) (603) and an electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$) (604), a source electrode (606) and a drain electrode (608) formed on the semiconductor layer structure while being separated from each other, a gate electrode (607) arranged between said source electrode and said drain electrode, and an insulating film (605a) formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion (above 605a) formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode (Fig. 6E; [0061-0067]).

Inoue does not teach the insulating film is a multilayered film including a first insulating film and a second insulating film, said first insulating film being made of a compound containing silicon and nitrogen as constituent elements, said second insulating film having a dielectric constant lower than that of said first insulating film.

Mayuzumi teaches the insulating film (9) is a multilayered film including a first insulating film (3) and a second insulating film (2 or 7), said first insulating film being made of a compound containing silicon and nitrogen as constituent elements, said second insulating film having a dielectric constant lower than that of said first insulating film to help form desired shape of the gate electrode due to the etching properties of the dielectrics (Fig. 4, 5, 8; [0017, 0033, 0034, 0043-0049]). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Inoue to have the multilayered film with the claimed properties to help form desired shape of the gate electrode due to the etching properties of the dielectrics as taught by Mayuzumi (Fig. 4, 5, 8; [0017, 0033, 0034, 0043-0049]).

Claim 2: Mayuzumi teaches the second insulating film is laminated on said first insulating film [0017].

Claim 3: Mayuzumi teaches the thickness of said first insulating film is not more than 150 nm [0033].

Claim 4: Mayuzumi teaches a dielectric constant of said second insulating film (7) is not more than 3.5 [0046].

Claim 8: Inoue teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including: a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) (603) and an electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$) (604), a source electrode (606) and a drain electrode (608) formed on the semiconductor layer structure while being separated from each other, a gate electrode (607) arranged between said source electrode and said drain electrode, and an

insulating film (605a) formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion (above 605a) formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode (Fig. 6E; [0061-0067]).

Inoue does not teach the insulating film is made of a compound containing silicon, nitrogen and oxygen as constituent elements. Mayuzumi teaches a insulating film is made of a compound containing silicon, nitrogen and oxygen as constituent elements (3) under a visored section of a gate electrode to help form desired shape of the gate electrode due to the etching properties of the dielectric (Fig. 4, 5, 8; [0017, 0033, 0034, 0043-0049]). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Inoue to have the constituent elements in the insulating film to help form desired shape of the gate electrode due to the etching properties of the dielectrics as taught by Mayuzumi (Fig. 4, 5, 8; [0017, 0033, 0034, 0043-0049]).

Claim 9: Inoue teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including: a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) (603) and an electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$) (604), a source electrode (606) and a drain electrode (608) formed on the semiconductor layer structure while being separated from each other, a gate electrode (607) arranged between said source electrode and said drain electrode, and an insulating film (605a) formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion (above 605a) formed on said insulating film while

said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode (Fig. 6E; [0061-0067]).

Inoue does not teach the insulating film has dielectric constant not more than 3.5. Mayuzumi teaches the insulating film (3) formed under a visored gate electrode has dielectric constants not more than 3.5 to help form desired shape of the gate electrode due to the etching properties of the dielectric (Fig. 4, 5, 8; [0017, 0033, 0034, 0043-0049]). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Inoue to have the insulating film with a dielectric constant not more than 3.5 to help form desired shape of the gate electrode due to the etching properties of the dielectric as taught by Mayuzumi (Fig. 4, 5, 8; [0017, 0033, 0034, 0043-0049]).

Claim 10: Inoue teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including: a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) (603) and an electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$) (604), a source electrode (606) and a drain electrode (608) formed on the semiconductor layer structure while being separated from each other, a gate electrode (607) arranged between said source electrode and said drain electrode, and an insulating film (605a) formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion (above 605a) formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode and said gate electrode side of said insulating film between said gate electrode and said drain electrode is made of

an insulating material (605a) having dielectric constants not more than 4 (Fig. 6E; [0061-0067]).

Inoue does not teach and said drain electrode side of said insulating film is made of an insulating material containing silicon and nitrogen as constituent elements. Mayuzumi teaches the insulating film between said gate electrode and said drain electrode is made of an insulating material (2 or 7) having dielectric constants not more than 4 and said drain electrode side of said insulating film is made of an insulating material (3) containing silicon and nitrogen as constituent elements to help form desired shape of the gate electrode due to the etching properties of the dielectric as taught by Mayuzumi (Fig. 4, 5, 8; [0017, 0033, 0034, 0043-0049]). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Inoue to have the drain electrode side of the insulating material containing silicon and nitrogen as constituent elements to help form desired shape of the gate electrode due to the etching properties of the dielectric as taught by Mayuzumi (Fig. 4, 5, 8; [0017, 0033, 0034, 0043-0049]).

Claim 11: Mayuzumi teaches the gate electrode side of said insulating film (7) is made of an insulating material containing silicon, nitrogen, and oxygen as the constituent elements (Fig. 4, 5, 8; [0017, 0033, 0034, 0043-0049]).

Claim 12: Inoue teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) (603) and an electron supply layer $Al_yGa_{1-y}N$ ($0 < y \leq 1$) (604), a source electrode (606) and a drain electrode (608) formed on the semiconductor layer

structure while being separated from each other, a gate electrode (607) arranged between said source electrode and said drain electrode, and an insulating film (605a) formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion (above 605a) formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode (Fig. 6E; [0061-0067]).

Inoue does not teach the drain electrode side is lower than said gate electrode side in a dielectric constant of a capacity formed by said field plate portion, said Group III nitride semiconductor layer, and said insulating film sandwiched therebetween, wherein a part of said insulating film is a multilayered film including a first insulating film and a second insulating film, said first film being made of a compound containing silicon and nitrogen as constituent elements, said second insulating film having a dielectric constant lower than that of said first insulating film, and said gate electrode side is formed by a single layer film of the first insulating film and said drain electrode side is formed by the multilayered film including said first insulating film and said second insulting film in said insulating film between said field plate portion and a surface of said semiconductor layer structure. Mayuzumi teaches the drain electrode side is lower than said gate electrode side in a dielectric constant of a capacity formed by said field plate portion, said Group III nitride semiconductor layer, and said insulating film sandwiched therebetween, wherein a part of said insulating film (2, 3, 7) is a multilayered film including a first insulating film (3) and a second insulating film (7), said first film being made of a compound containing silicon and nitrogen as constituent elements, said

second insulating film having a dielectric constant lower than that of said first insulating film, and said gate electrode side is formed by a single layer film of the first insulating film and said drain electrode side is formed by the multilayered film (2, 3, and 7) including said first insulating film (3) and said second insulting (7) film in said insulating film between said field plate portion and a surface of said semiconductor layer structure

Claim 18: Inoue teaches a semiconductor layer structure has a structure in which the channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$), the electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$), and a cap layer made of GaN are sequentially laminate [0050]. Inoue does teach these layers are sequentially laminate, however, it is noted that "The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made.

Claim 22: Inoue teaches the field plate portion having a visored shape does not overhang any part of said insulating film between said gate electrode and said source electrode (Fig. 6E; [0061-0067]).

Claim 23: Inoue teaches the field plate portion having a visored shape does not overhang any part of said insulating film between said gate electrode and said source electrode (Fig. 6E; [0061-0067]).

9. Claims 5, 6 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (US PGPub 2001/0015446 of record) and of Mayuzumi (US PGPub 2002/0079525) as applied to claim 1 above, and further in view of Mizuta et al. (US Patent 6,483,135 of record).

Regarding claim 15, as described above, Inoue and Mayuzumi substantially read on the invention as claimed, except Inoue and Mayuzumi do not teach the contact layers are arranged between said source electrode and a surface of said semiconductor layer structure and between said drain electrode and a surface of said semiconductor layer structure, respectively. Mizuta teaches the contact layers (3) are arranged between said source electrode (7/8) and a surface of said semiconductor layer (2) structure and between said drain electrode (7/8) and a surface of said semiconductor layer structure, respectively to improve device performance (FIG. 7; Col. 1). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Inoue and Mayuzumi to have the contact layers between the source/drain electrodes and the semiconductor layer to improve device performance as taught by Mizuta (FIG. 7; Col. 1).

Claim 5: Mizuta teaches said insulating film including said multilayered film is formed while being separated from said gate electrode, and said second insulating film (4a) is provided between said first insulating film (4b) and said gate electrode (5) (FIG. 9e).

Claim 6: Mizuta teaches said second insulating film (4a) is provided between said first insulating film (4b) and said gate electrode (5) and said second insulating film

is positioned below said field plate portion (5 above 4a and 4b), and said multilayered film including said first insulating film and said second insulating film is positioned between a drain-side end portion of said field plate portion and said drain electrode (FIG. 9f).

10. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (US PGPub 2001/0015446 of record) and Mayuzumi (US PGPub 2002/0079525), as applied to claim 1 above, and further in view of Parikh et al. (US PGPub 2003/0020092).

Regarding claim 7, as described above, Inoue and Mayuzumi substantially read on the invention as claimed, except Inoue and Mayuzumi do not teach a third insulating film on said second insulating film, the third insulating film being made of a compound containing silicon and nitrogen as the constituent elements. Parikh teaches adding an additional dielectric layer of SiN on the surface of the existing insulating layers to further protect the device from passivation and impurities that can damage the device during handling [0038]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Inoue and Mayuzumi to include a third dielectric layer of SiN to further protect the device from passivation and impurities that can damage the device during handling as taught by Parikh [0038].

11. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (US PGPub 2001/0015446 of record), Mayuzumi (US PGPub 2002/0079525) and Mizuta et al. (US Patent 6,483,135 of record) as applied to claim 15 above, and further in view of Sheppard et a. (US Patent 2001/0017370 of record).

Regarding claim 16, as described above, Inoue, Mayuzumi and Mizuta substantially read on the invention as claimed, except Inoue, Mayuzumi and Mizuta do not teach a contact layer formed by an undoped AlGaN. Sheppard teaches an undoped AlGaN contact layer (17) to improve the characteristics of the device [0011, 0026]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Inoue, Mayuzumi and Mizuta to make the contact layer out of undoped AlGaN to improve the characteristics of the device as taught by Sheppard [0011, 0026].

Claim 17: Mizuta teaches the field plate portion extends to an upper portion of said contact layer (FIG. 7).

12. Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (US PGPub 2001/0015446 of record) in view of Mayuzumi (US PGPub 2002/0079525) and Hirokawa (US PGPub 2002/0043697 of record).

Claim 19: Claim 1: Inoue teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) (603) and an electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$) (604), a source electrode (606) and a drain electrode (608) formed on the

semiconductor layer structure while being separated from each other, a gate electrode (607) arranged between said source electrode and said drain electrode, and an insulating film (605a) formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion (above 605a) formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode (Fig. 6E; [0061-0067]).

Inoue does not teach the insulating film is a multilayered film including a first insulating film and a second insulating film, said first insulating film being made of a compound containing silicon and nitrogen as constituent elements, said second insulating film having a dielectric constant lower than that of said first insulating film. Mayuzumi teaches the insulating film (9) is a multilayered film including a first insulating film (3) and a second insulating film (2 or 7), said first insulating film being made of a compound containing silicon and nitrogen as constituent elements, said second insulating film having a dielectric constant lower than that of said first insulating film to help form desired shape of the gate electrode due to the etching properties of the dielectrics (Fig. 4, 5, 8; [0017, 0033, 0034, 0043-0049]). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Inoue to have the multilayered film with the claimed properties to help form desired shape of the gate electrode due to the etching properties of the dielectrics as taught by Mayuzumi (Fig. 4, 5, 8; [0017, 0033, 0034, 0043-0049]).

Inoue and Mayuzumi do not teach the size of said field plate is not lower than 0.3μm. Hirokawa teaches a size of said field plate is not lower than 0.3μm to improve

device performance (Abs, [0026]). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have specified the field plate length of Inoue and Mayuzumi to be not lower than .3 μm to improve device performance as taught by Hirokawa (Abs, [0026]).

Claim 20: Hirokawa teaches a size of said field plate is not lower than 0.5 μm.

Claim 21: Hirokawa teaches a size of said field plate portion is not more than 70% of a distance between said gate electrode and said drain electrode.

Response to Arguments

13. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SARAH K. SALERNO whose telephone number is (571)270-1266. The examiner can normally be reached on M-R 8:00-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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